equivalents thereof. Accordingly, the aim in the appended claims is to cover all such changes and modifications as fall within the true spirit and scope of the invention.

The Invention is claimed as follows:

1. A pseudo-random communication system in which a transmitter-generated encoded signal is to be correlated with a receiver-generated similarly encoded signal for recognizing synchronization of the transmitted and received signals in the presence of undesired received energy, said system comprising: a spread-spectrum transmitter including at least two pseudo-noise generators for producing at least two pseudo-noise signals which are related by a ratio slightly removed from unity mixing means for receiving and mixing said two pseudo-noise signals with respective carrier and information signals to produce an output signal, and means for transmitting the output signal; and a spread-spectrum receiver comprising correlator means and matched filter means coupled in circuit to form synchronization detector circuit means for receiving and detecting the encoded output signal transmitted by said transmitter means so as to recover the information therefrom; said correlator means including at least one pseudo-noise generator means for producing pseudo-noise signals related in a predetermined fashion to the pseudo-noise signals produced by the transmitter pseudo-noise generators and mixer means for mixing said pseudo-noise signals with the received encoded output signals and coupled in circuit with said matched filter circuit means.

2. A system according to claim **1** wherein said transmitter circuit means further comprises a first mixer coupled to receive and mix the pseudo-noise signals from said at least two pseudo-noise generators with a carrier signal to provide a first mixer signal, and a second mixer circuit coupled to receive and mix said first mixer signal with an information signal to provide said encoded output signal.

3. A system according to claim **1** wherein said correlator means comprises a sliding correlator comprising at least one pseudo-noise generator for producing said pseudo-noise signal in accordance with a clock signal input applied thereto, and further including clock controller circuit means for producing said clock signal input for said pseudo-noise generator.

4. A system according to claim **1** wherein said matched filter circuit means comprises a bandpass filter circuit and a SAW correlator circuit.

5. A system according to claim **1** wherein said synchronization detector circuit means comprises a correlator circuit means including at least two pseudo-noise generator circuits, and associated mixer circuits and clock controller circuit means for producing clock signals for driving each of said two pseudo-noise generator circuits; said clock controller circuit means being coupled in circuit for producing respective clock signals in response to predetermined output signals of said matched filter circuit means.

6. A system according to claim **5** wherein the output of at least one of said mixer circuits is coupled in circuit for driving said matched filter circuit means; said second mixer circuit being coupled in circuit providing a decoded signal output for further processing by further radio receiving circuit means.

7. A system according to claim **3** wherein said clock controller circuit means comprises a voltage controlled oscillator for producing an output signal having a frequency determined by the voltage of an input signal applied thereto; a voltage controlled delay circuit coupled to said voltage controlled oscillator circuit for applying a time delay to the oscillator output signal determined by a second control voltage applied thereto; sources of first and second control voltages for said voltage controlled oscillator and switching means for selecting between said first and second control voltages; source of a third, selectable control voltage coupled for applying the same to said voltage controlled delay circuit; voltage summing circuit means coupled intermediate one of said first and second control voltage sources and said switching means; and weighting circuit means coupled intermediate said third control voltage source and said summing circuit means.

8. A system according to claim **7** wherein said switching means comprises a controllable switching means responsive to synchronization detection in said receiver circuit for switching between said first and second control voltages for application to said voltage-control oscillator, said first control voltage comprising a base voltage for controlling a sliding correlation circuit and said second control voltage comprising a voltage to hold said sliding correlation circuit in synchronization following synchronization detection.

9. A system according to claim **8** wherein said third control voltage, applied to said voltage-controlled delay circuit, comprises a ramp voltage signal.

10. A system according to claim **1** wherein said receiver circuit means further comprises modulation code correlator threshold controller circuit means comprising oscillator circuit means for producing an oscillatory output signal at a selected frequency; summing circuit means; filter circuit means coupled to receive said oscillator circuit output signal; threshold circuit means coupled to receive an output of said correlator means and the summed output of said summing circuit means as a threshold control signal; multivibrator circuit means coupled intermediate a threshold output voltage of said threshold circuit and an input of said filter circuit; an output of said filter circuit being used as a low signal level warning signal and also being fed back to an input of said summing circuit means.

11. A system according to claim **3** wherein said receiver circuit further includes a modulator code correlator signal inhibit circuit comprising a selectively activatable correlator signal inhibitor circuit and a time counting circuit responsive to a single correlator signal entry for activating said correlator signal inhibitor following a predetermined time delay.

12. A method for producing a pseudo-noise signal for use in transmitting and receiving encoded signals in a pseudo-random communication system, said method comprising: producing at least two pseudo-noise signals which are related in a predetermined fashion, said two different pseudo-noise signals having a predetermined relationship between their chip rates, said chip rates thereof being related by ratio slightly removed from unity, and combining said two pseudo-noise signals in a predetermined fashion to form a composite signal for use in encoding and decoding information in said pseudo-random communications system.

13. A method according to claim **12** wherein the two pseudo-noise signals are 15-bit length M-series codes and wherein clocks are used for chip timing of the two pseudo-noise rates, said clocks having a frequency ratio of substantially 29/30.